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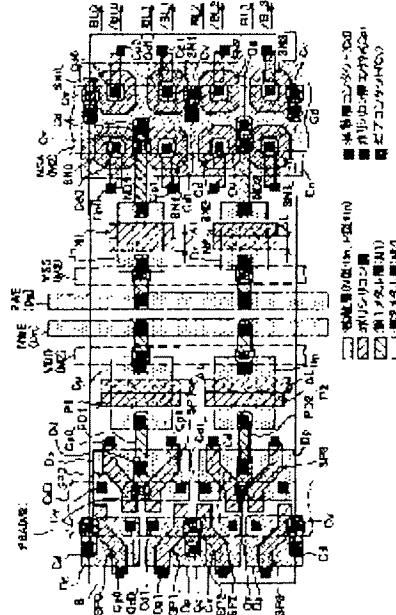
## (54) SEMICONDUCTOR MEMORY DEVICE

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To provide a semiconductor memory device which is furnished with driver transistors for power supply, wherein power supply capability to sense amplifiers is kept during the activated state while the leakage current is reduced during the non-activated state.

**SOLUTION:** PMOS transistors P1, P2 and NMOS transistors N1, N2 for a driver supply power source voltage VDD and reference voltage VSS to PMOS transistors SP0, SP0- to SP3, SP3-, and NMOS transistors SN0, SN0- to SN3, SN3-, and are arranged with the gate-width directions perpendicular to the bit-line direction on every two pitches of a bit-line pair. The gate widths of the PMOS transistors P1, P2 and the NMOS transistors N1, N2 are adjusted within the maximum value of two pitches of the bit-line pair, while the gate lengths are adjusted within an adjustable range  $\Delta L$ . Consequently, MOS transistors P1, P2, N1, and N2 for the driver that have been properly adjusted for contradicting characteristics of keeping current supply capability and reducing the tailing current, are obtained.

本発明の実施形態におけるセンスアンプブロック内の  
センスアンプ領域についてのレイアウト構成



## LEGAL STATUS

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